AMENDMENTS

IN THE SPECIFICATION

1) page 6, last paragraph, pleased replace this paragraph with the following text:

The brief description of the process of metallization that has been given above has been described with reference to the damascene and dual damascene processes which are two widely used approaches in creating metal interconnects. The application of the damascene process has gained wide acceptance in the semiconductor industry, most notably in the process of copper metallization due to the difficulty of copper dry etch where the damascene plug penetrates deep in very small, sub-half micron, Ultra Large Scale Integrated (ULSI) devices. Recent applications have successfully used copper as a conducting metal, most notably in the construct of CMOS 6-layer copper metal devices.

2) page 7, second paragraph, pleased replace this paragraph with the following text:

The damascene process first etches the conductor pattern into the dielectric after which the etched pattern is filled with metal to create the buried metallization that also has a surface of good planarity. This damascene process also eliminates the need of a dielectric deposition in order to fill the gaps. A planarized metal deposition process can be used for this to fill the pattern that has been created in a dielectric layer of for instance SiO_2. An etchback or CMP process will remove the excess metal over the field regions, CMP thereby offers the advantage of providing a globally planarized surface. The indicated processing steps can be applied to both single and dual damascene.

3) page 7, second paragraph, pleased replace this paragraph with the following text:

Fig. 1c shows a cross section after the layer 12 has been etched in accordance with the photoresist mask 14. A layer 16 of residue of layers 12 and 14 remains in place inside opening 17 after the layer of photoresist has been exposed and developed and after opening 17 has been created through layer 12 of dielectric. It is clear that layer 16 interferes with subsequent deposition of conductive material over the surface of layer 12. This conductive material, typically metal, fills opening 17 and serves as an

interconnect plug forming for instance the via plug or the trench section of a dual damascene structure.

4) page 15, second paragraph, pleased replace this paragraph with the following text:

In a typical application of which the cross-sections that are shown in Figs. 1a through 1c are representative examples, an etch stop layer is formed over the surface of layer 10. This etch stop layer retards the etch of layer 12 in order to prevent damage to the surface of silicon substrate 10 and provides the end of the etch through layer 12. Multiple etch stop layers may also be applied for applications where multiple layers of dielectric are used for the creation of a dual damascene structure with for instance an etch stop layer being interspersed between a first (or lower) layer of dielectric and a second (or upper) layer of dielectric. These aspects of creating a dual damascene structure will not be discussed as part of the invention.

5) page 16, second paragraph, pleased replace this paragraph with the following text:

The invention will now specifically be described using Figs. 2a through 2g. Referring specifically to the cross section that is shown in Fig. 2a, there are highlighted the following elements:

- 10, the surface of a silicon substrate, active devices (not shown) are assumed to have been created in or on the surface of the substrate
- 22, a layer of Inter Metal Dielectric (IMD)
- 24, an opening created through the layer 12 of IMD. Opening 12 through the layer 12 has been created preferably applying a wet etch process.

6) page 16, last paragraph, pleased replace this paragraph with the following text:

The creation of opening 24 through the layer 22 of IMD is a step that is part of a complete processing sequence of creating a damascene or a dual damascene structure although the creation of opening 24 is not limited to damascene structures. Conventional methods of semiconductor material deposition, photolithography and dielectric etching have been applied in order to create the structure that is shown in cross section in Fig. 2a. The opening 24 shown in Fig. 2a is an opening for the creation of an I-line plug for devices having deep sub-micron dimensions.

7) page 18, last paragraph, page 19, first paragraph, pleased replace this paragraph with the following text:

It is clear and has previously been highlighted that the formation of layer 29 must be prevented. The invention provides, for this purpose, a processing step that is performed after the completion of the structure that is shown in cross section in Fig. 2c, that is after the I-line layer of photoresist has been etched back and a significant portion of the sidewalls of opening 24, Fig. 2c, is exposed. At that time, that is after the processing step that results in the cross section shown in Fig. 2c and before the processing step of Fig. 2d of depositing layer of DUV photoresist, a baking step is added to the processing cycle. This baking step removes moisture from the layer 22 of IMD so that this moisture is no longer present during the step of etching the layer 28 of DUV photoresist, thus removing a key contributor to the formation of scum photoresist layer 29 of Fig. 2e. By then performing the steps of depositing layer 28 of DUV photoresist (Fig. 2d) and developing of the layer 28 of DUV photoresist, no layer of photoresist scum is formed and a cross section that is shown in Fig. 2f is achieved. From this cross section it is clear that the now familiar cross section of a dual damascene structure has been formed in the opening 32 that has been formed through layers 28 and 22 of respectively DUV photoresist and IMD. Layer 26 of I-line